

CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a device isolation layer formed at a predetermined region, the device
isolation layer defining a cell active region, a resistor active region, and an
MROM active region;

a resistive junction region formed in the resistive active region;

a covering gate crossing the resistive junction region and the device
isolation layer;

a channel junction region formed in the MROM active region;

a memory gate and a select gate crossing the cell active region and the
device isolation layer; and

a floating junction region formed in the cell active region under the
memory gate,

wherein the floating junction region, the resistive junction region, and
the channel junction region have the same depth.

2. The device as claimed in claim 1, comprising a first gate oxide
layer disposed under the covering gate, the select gate, and the memory gate.

3. The device as claimed in claim 2, comprising a tunnel oxide
layer disposed under the memory gate, the tunnel oxide layer being surrounded
by the first gate oxide layer.

4. The device as claimed in claim 3, wherein a thickness of the tunnel oxide layer is less than that of the first gate oxide layer.

5 5. The device as claimed in claim 2, wherein a second gate oxide layer, having a thickness less than that of the first gate oxide layer, is disposed under the MROM gate.

6. The device as claimed in claim 1, wherein the memory gate
10 includes a floating gate, a gate interlayer insulation layer, and a control gate, which are sequentially stacked.

7. The device as claimed in claim 1, wherein the select gate
includes a lower select gate, a select gate interlayer insulation layer, and an
15 upper select gate, which are sequentially stacked.

8. The device as claimed in claim 1, wherein layers constituting the select gate are the same material layers as layers constituting the memory gate.

20 9. The device as claimed in claim 1, wherein layers constituting the covering gate are the same material layers as layers constituting the select gate.

10. The device as claimed in claim 6, wherein the MROM gate is the same material layer as the control gate.

5 11. The device as claimed in claim 1, wherein the floating junction region, the resistive junction region, and the channel junction region include the same impurities.

10 12. The device as claimed in claim 1, wherein the floating junction region, the resistive junction region, and the channel junction region have the same impurity concentration.

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